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(54) Structure and method for use in a semiconductor field oxidation process.

(57) In a process for forming field oxide regions (40) between active regions in a semiconductor substrate (10), pad oxide, polysilicon and first silicon nitride layers (12,14,16) are successively formed over substrate active regions. The first nitride layer (16), polysilicon layer (14), pad oxide layer (12) and a portion of the substrate (10) are then selectively etched to define field oxide regions with substantially vertical sidewalls (21). A second silicon nitride (32) is provided on the substantially vertical sidewalls (21), and field oxide (40) is grown in the field oxide regions. The first silicon nitride, polysilicon and pad oxide layers (16,14,12) are then removed. The employment of the polysilicon layer (14) prevents the exposure of corners (44) between the field oxide (40) and active regions if an overetch occurs during the removal of the pad oxide layer (12).

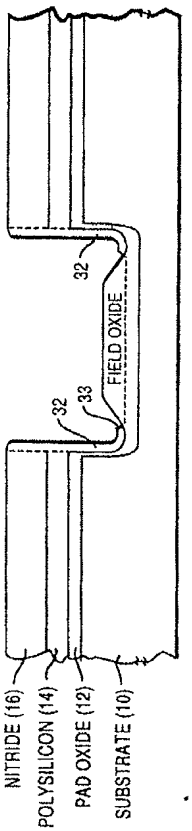

FIG. 5

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This invention relates to a structure and method for use in a semiconductor field oxidation process, applicable in the manufacture of integrated circuits.

The fabrication of an integrated circuit normally begins by processing the semiconductor substrate or wafer to divide the surface area into regions where active devices and substrate embedded interconnects are to be formed, and other regions of dielectric which electrically separate the active regions. The field oxide dielectric material is routinely silicon dioxide. Though various field oxide formation techniques have been developed and described, the technique commonly known as the localized oxidation of silicon (LOCOS) remains common within the semiconductor industry. In the practice of LOCOS, the active regions of the silicon substrate are masked by a silicon nitride layer, while the field oxide regions are thermally oxidized to form a field dielectric region. Though fundamentally simple and efficient, the LOCOS process, and its progeny, such as the FUROX and SWAMI techniques, exhibit deficiencies which reduce yield or performance in the final semiconductor chip product.

The most frequently encountered deficiency in the prior art techniques is commonly known as the bird's beak problem, wherein the field oxide extends under the masking nitride layer to consume some of the usable active area. Additional problems routinely encountered with known field oxide formation processes include stress induced dislocations at the edges of the active region, and the presence of a relatively nonplanar surface in or adjacent the fully formed field oxide. The nonplanar recesses or notches at the edges of the active region often degrade subsequently formed gate oxide, which can trap conductive layer residuals creating short circuit paths. Solutions to these problems have been proposed, but routinely involve relatively complex or dimensionally critical fabrication sequences which are costly to practice or degrade the semiconductor chip yield.

Though a number of techniques successfully attack and solve the bird's beak problem, and usually provide relatively planar final concluding surfaces, the approaches routinely create stress induced dislocations at the edges of the active regions, and form topologies which include notches or grooves of sufficient dimension to cause the degradation of subsequently formed gate oxide. The stress induced dislocations are often not even recognized, while the notches or grooves are most often visible in the SEM cross-sections of the final structures.

A process which overcomes many of the problems encountered by the earlier processes is known as recessed sealed sidewall field oxidation (RESSFOX). One form of the RESSFOX process is disclosed in U.S. Patent No. 4,923,563. In brief, the RESSFOX process utilizes a relatively thick pad oxide below a first masking nitride layer. A second, very thin, masking nitride layer is applied to the sidewall of an etched opening to define the lateral boundaries of a field oxide region. The thin sidewall masking nitride layer does not utilize an underlying pad oxide layer although it may include a thin underlying screening oxide. Upon oxidation, the thin sidewall nitride is concurrently lifted and converted to oxide, the materials and dimension being selected to ensure that when the field oxide level approaches the level of the thick pad oxide layer stresses at the corners of the active silicon region are relieved through various oxide paths and accentuated-oxidation effects.

After the field oxide growth, and in preparation for the formation of active devices, the substrate in the active regions is exposed. This is achieved by removing a topmost oxidized nitride layer (formed during the field oxide growth), such as by etching with HF. The first masking nitride layer is then removed with an acid such as a hot H_3PO_4, and the pad oxide is removed by a chemical (HF) etch. Of course, a portion of the field oxide is also removed each time an oxide layer is removed by a chemical etch. If the etching chemical remains too long on the surface of the chip, overetching of the field oxide occurs and a corner of the substrate may be exposed on the boundary of the field oxide region. The gate oxide for the active devices is then grown on the surface of the resulting structure. Under carefully controlled processing, the structure underlying the gate oxide is well suited for gate oxide growth. However, if corners are exposed by overetching, a thinning of the subsequently grown gate oxide can occur which can create integrity/reliability problems for the resulting chip.

It is an object of the present invention to provide a structure and method for forming a semiconductor integrated circuit device which enable processing criticality to be reduced.

Therefore, according to one aspect of the present invention, there is provided a structure for fabricating an integrated circuit, including a silicon substrate and a pad oxide layer overlying said substrate, characterized by a polysilicon layer overlying said pad oxide layer; a first nitride layer overlying said polysilicon layer; an opening through said first nitride polysilicon and pad oxide layers and into said silicon substrate defining a region for field oxide growth, having a sidewall surface and an adjoining bottom surface; and a second nitride layer overlying said sidewall surface.

According to another aspect of the present invention, there is provided a process for forming field oxide regions between active regions in a semiconductor substrate, including the step of forming over said active regions a pad oxide layer, characterized by the steps of forming over said pad oxide layer a polysilicon layer; forming over said polysilicon layer a first silicon nitride layer; selectively etching through said first nitride layer said polysilicon layer and said pad oxide layer, and into said substrate to define field

oxide regions having sidewalls; providing a second silicon nitirde layer on said sidewalls; growing field oxide in said field oxide regions; and removing said first silicon nitride, polysilicon and pad oxide layers.

It will be appreciated that a structure and method according to the invention reduce processing criticality by enabling the avoidance of the exposure of corners between the field oxide and active regions if an overetch occurs during removal of the pad oxide layer.

One embodiment of the present invention will now be described by way of example, with reference to the accompanying drawings, in which:-

Figures 1-4 are cross-sectional schematic representations of an integrated circuit substrate at various stages in the fabrication sequence prior to field oxide growth;

Figures 5-7 schematically illustrate, in cross-section, progressive stages of the field oxide growth;

Figures 8-9 schematically illustrate, in cross-section, selected stages leading up to and including the formation of gate oxide; and

Figure 10 is a cross-sectional schematic representation of an overetch of the field oxide.

Figure 1 shows a silicon substrate 10, a pad oxide layer 12 overlying substrate 10, a polysilicon layer 14 overlying pad oxide layer 12, a silicon nitride layer 16 overlying polysilicon layer 14, and topped off with a patterned photoresist 18. To create the structure in Figure 1, the silicon substrate 10 is first thermally oxidized to form pad oxide layer 12 having a nominal thickness of 5-100 nanometers.

As further shown in Figure 1, pad oxide 12 on substrate 10 is then covered by polysilicon layer 14, formed to a nominal thickness of 3-100 nm by chemical vapor deposition (CVD) process or the like. In the prior art, polysilicon layers are frequently used for stress relief purposes. However, the RESSFOX process does not require stress relief at this point. Polysilicon layer 14 serves the quite distinct purpose of preventing a sharp corner between the active and field oxide regions from being exposed in the event of an overetch, as will be discussed more fully herein.

The silicon nitride I layer 16 is preferably formed to a nominal thickness of 10-500 nm by LPCVD. In preparation for a selective etch, photoresist 18 is deposited and photolithographically processed to retain a photoresist (PR) mask pattern exposing nitride I layer 16 at opening 20, generally corresponding to the field oxide formation region between active regions 22 in substrate 10.

To reach the stage of fabrication depicted in Figure 2, the structure in Figure 1 is anisotropically etched using a conventional reactive ion etching (RIE) process to remove nitride I layer 16 not masked by photoresist 18, the aligned segment of polysilicon 14 and pad oxide layer 12, and a section of substrate 10 suitable to form a recess between 30 and 150 nanometers deep into substrate 10. The opening 20 created by the selective etch through nitride layer 16, polysilicon layer 14, pad oxide layer 12 and into substrate 10 defines a region for field oxide growth, as will be described in more detail as follows. Opening 20 is bounded by vertical sidewall surface 21 and a horizontal adjoining bottom surface 30. Preferably, sidewall surface 21 is normal to bottom surface 30 as well as each of the pad oxide 12, polysilicon 14 and nitride 16 layers. Photoresist 18 is next stripped, and a field implant may be performed, for example, to provide a channel stop for an NMOS transistor. This implant is done by doping selected regions of the substrate through selected horizontally disposed surfaces of the substrate prior to the growth of field oxide in opening 20. In a CMOS device the field oxide will separate NMOS and PMOS transistors. For such device the PMOS side of opening 20 is masked with photoresist 24 prior to the field implant in the NMOS side. Because photoresist materials typically include elements which may contaminate substrate 1, and because photoresist adhesion to silicon is relatively poor, a thin screening oxide layer 26 may be formed on the sidewalls over the substrate and pad oxide layer prior to the application of the photoresist to prevent contamination during field implantation. Screening oxide 26 with nominal thickness of less than 20nm and preferably about 10nm may be thermally grown on bottom surface 30 and sidewall 21, followed by the application of photoresist 24. After the field implant, photoresist 24 is removed. Screening oxide 26 may also be removed. However, since screening 26 oxide is so thin, it is not necessary to remove it prior to further processing. It has been found that the presence of screening oxide 26 does not degrade the process, i.e., the screening oxide is sufficiently thin so that there is no significant increase in lateral encroachment during field oxide growth.

As shown in Figure 3, a second silicon nitride II layer 28 is deposited by an LPCVD process to conformally cover the structure. The structure is then subjected to another anisotropic etch, this etch serving to remove the silicon nitride from exposed horizontal surfaces. As a consequence of such anisotropic etch, as shown in Figure 4, the bottom surface 30 of the recess at opening 20 in silicon substrate 10 is exposed to the substrate silicon, while sidewall silicon nitride II layer 32 (which overlies sidewall surface 21) is retained but thinned by a nominal amount.

Note that at most only a nominal amount of screening oxide is disposed between sidewall 21 and sidewall nitride 32, thereby inhibiting the movement of oxygen species along the underside of sidewall nitride layer 32 during thermal field oxide growth. Clearly, oxygen species are also blocked from direct access to pad oxide layer by sidewall nitride layer 32 during the initial stages of field oxide growth. The dimensions of sidewall nitride layer 32 are relatively crucial, not

only in controlling the oxidation effects, but also in avoiding coefficient of expansion differential induced stress damage along sidewalls 34 of silicon substrate 10. Namely, sidewall nitride 32 is sufficiently thin at 25 nm or less to yield rather than cause stress damage to silicon substrate 10. Sidewall 34 is oxidized at a rate suitable to facilitate bending and lifting with silicon dioxide growth, yet is sufficiently thick to block oxidizing species' access to the pad oxide region until the specifically desired time. In a preferred embodiment, nitride II layer 32 has a nominal thickness of 5-25 nm.

Figures 5-7 depict the structure at various stages in the growth of the field oxide. The exposed substrate 10 and sidewall nitride 32 is oxidized in a proportion to effectuate concurrent oxidation and lifting and bending, beginning at the low edge 33 of the retained sidewall silicon nitride 32. The field oxide growth uses a preferred field oxidation environment of $H_2 + O_2$, at a nominal temperature of approximately 900:C for a nominal time of 750 minutes. Alternatively, a field oxidation environment of either a dry O_2 or $H_2 + O_2$, at a pressure of about 10 atm and a nominal temperature of about 875°C, for about 120 minutes may be employed. As the field oxide growth continues in progressing to the structure shown in Figure 6, the former sidewall nitride layer 32 is fully lifted and bent. During this time, stress in sidewall regions 36 of silicon substrate 10 is relieved by the presence of the thin sidewall nitride at the commencement of oxidation and its further thinning by surface conversion to oxide during oxidation. At the stage of oxidation depicted in Figure 6, nitride layers 38 would be thinned to approximately 3 nm or less.

Figure 6 also illustrates that the lifting of the residual sidewall silicon nitride 38 exposes the relatively thick pad oxide 12 and polysilicon layer 14 near the end of oxidation. Pad oxide 12 then serves as a path for relieving volumetric increase stresses in field oxide 40 proximate silicon substrate corners 42, corners which otherwise would be likely to encounter stress induced dislocations. As the field oxide growth continues into the final stage depicted in Figure 7, conversion of residual sidewall silicon nitride 38 to oxide opens a relatively short path for oxygen species to reach silicon substrate corners 42. The result is an accentuated oxidation rate at silicon substrate corners 42 to create corners 44 of relatively large radius, smooth contour, and reduced local stress. Again, the relatively thick pad oxide layer 12 provides a yielding path for the relief of localized stresses, which path supplements the vertically directed movement and relief in the region 46. Furthermore, the relatively limited growth of field oxide 40 over the lower corner regions 48 of nitride layer 16, by virtue of the masking by sidewall nitride layer 38 (Figure 6), substantially suppresses the formation of notches or grooves in the field oxide at the edges of the active regions 22. The oxidation of the substrate and lifting of the sidewall silicon nitride continues and is complemented by an oxidation of polysilicon 16 until the upper surface of the oxidized substrate reaches a predetermined level, which in a preferred embodiment is at least as high as the interface between polysilicon layer 14 and nitride layer 16.

As a consequence of the balanced interaction between the lifting and bending of the sidewall nitride layer, the conversion of the sidewall nitride to an oxide, the relief of stress through the pad oxide, the accentuated conversion of the polysilicon at the edge of the active region near the conclusion of the oxidation step, and the multidirectional relief of stresses at the relatively rounded corners of the active regions, not only is the bird's beak problem substantially suppressed, but the active region does not experience stress induced dislocations nor does the structure of the field oxide incorporate deleterious notches or grooves.

Figure 8 illustrates a representative integrated circuit structure, following the removal of a top layer of oxidized nitride (not shown) (formed during field oxide growth), the masking nitride 16 (Figure 7), polysilicon layer 14 and pad oxide layer 12. In a preferred embodiment, both the oxidized nitride coating and pad oxide layer 12 are removed by chemical (HF) etching. Such etching is difficult to accurately control and overetching of the oxide can easily occur. In the previous RESSFOX process described in U.S. Patent 4,923,563, if an overetch of the field oxide occurred, corners 44 of substrate 10 could be exposed. Reliability problems can be created when a subsequent gate oxide is formed over corners 44. A primary purpose of polysilicon layer 14 is to increase the thickness of the field oxide above the bird's beak thereby preventing corners 44 from becoming exposed in the event of an overetch. In this manner the criticality of the etching step is reduced.

Figure 9 shows the integrated circuit structure after forming a gate oxide layer 50 in preparation for the formation of active devices.

Figure 10 is a view similar to Figure 8, but illustrating the structure following an inadvertent overetch of pad oxide layer 12. It should be noted that the dip 52 in field oxide 40 caused by the overetch does not expose corners 44.

Claims

1. A structure for fabricating an integrated circuit, including a silicon substrate (10) and a pad oxide layer (12) overlying said substrate (10), characterized by a polysilicon layer (14) overlying said pad oxide layer (12); a first nitride layer (16) overlying said polysilicon layer (14); an opening (20) through said first nitride (16) polysilicon (14) and

pad oxide (12) layers and into said silicon substrate (10) defining a region for field oxide growth, having a sidewall surface (21) and an adjoining bottom surface (30); and a second nitride layer (32) overlying said sidewall surface (21).

2. A structure according to claim 1, characterized in that said polysilicon layer (14) has a nominal thickness of 3-100 nm, said pad oxide layer (12) has a nominal thickness of 5-100 nm, said first nitride layer (16) has a nominal thickness of 10-500 nm, and said second nitride layer (32) has a nominal thickness of 5-25 nm.

3. A structure according to claim 1, characterized in that said sidewall surface (21) is substantially normal with respect to said bottom surface (30).

4. A structure according to any one of the preceding claims, characterized in that a thin screening oxide layer (26) is disposed between said sidewall surface (21) of said opening (20) and said second nitride layer (32).

5. A structure according to claim 4, characterized in that said screening oxide layer (26) has a thickness of less than 20 nm.

6. A structure according to any one of the preceding claims, characterized in that said opening (20) within said substrate (10) is between 30 and 150 nm.

7. A process for forming field oxide regions between active regions in a semiconductor substrate (10), including the step of forming cover said active regions a pad oxide layer (12), characterized by the steps of forming over said pad oxide layer (12) a polysilicon layer (14); forming over said polysilicon layer (14) a first silicon nitride layer (16); selectively etching through said first nitride layer (16), said polysilicon layer (14) and said pad oxide layer (12), and into said substrate (10) to define field oxide regions having sidewalls (21); providing a second silicon nitride layer (32) on said sidewalls (21); growing field oxide (40) in said field oxide regions; and removing said first silicon nitride, polysilicon and pad oxide layers (16,14,12).

8. A process according to claim 7, characterized by the step of forming a gate oxide layer (50) over the structure remaining after removing said first silicon nitride, polysilicon and pad oxide layers (16,14,12).

9. A process according to claim 7 or 8, characterized in that said field oxide (40) is grown by the steps of: oxidizing the exposed substrate (10) and second silicon nitride (32) in a proportion to effectuate concurrent oxidation and lifting and bending, beginning at the low edge of the retained sidewall silicon nitride (32); and continuing the oxidation of the polysilicon (14) and substrate (10) and the lifting of the sidewall silicon nitride (32) until the upper surface of the oxidized substrate reaches a predetermined level.

10. A process according to any one of claims 7 to 9, characterized by the steps of, prior to providing said second silicon nitride layer (32), forming a relatively thin screening oxide layer (26) on said sidewalls (21); and doping selected regions of said substrate (10) through selected horizontally disposed surfaces of said substrate (10) underlying said field oxide regions.

11. A process according to any one of claims 7 to 10, characterized in that said step of providing said second silicon nitride layer (32) includes the steps of: forming a conformal second silicon nitride layer (28), over the patterned structure of the substrate and layers, including the substantially vertical sidewalls (21), to a nominal thickness of less than 25 nm; and removing the horizontally disposed second silicon nitride layer (28) to expose horizontally disposed surfaces (30) of said substrate (10), while retaining a second silicon nitride layer (32) on the said sidewalls (21).

12. A process according to any one of claims 7 to 11, characterized in that said polysilicon layer (14) is formed to a nominal thickness of 3-100 nm, said pad oxide layer (12) is formed to a nominal thickness of 5-100 nm, and said first nitride layer (16) is formed to a nominal thickness of 10-500 nm, and in that the depth of the etch into said substrate (10) is between 30 and 150 nm.

13. A process according to any one of claims 7 to 12, characterized in that said field oxide (40) is grown to a level at least as high as the interface between said polysilicon layer (14) and said first nitride layer (16).

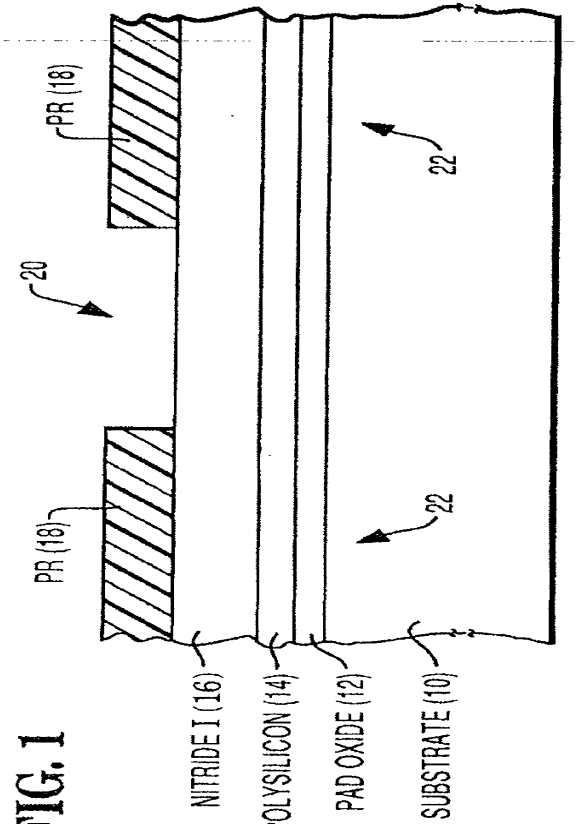

PR (18)
20
PR (18)
22
22
NITRIDE I (16)
POLYSILICON (14)
PAD OXIDE (12)
SUBSTRATE (10)

FIG. 1

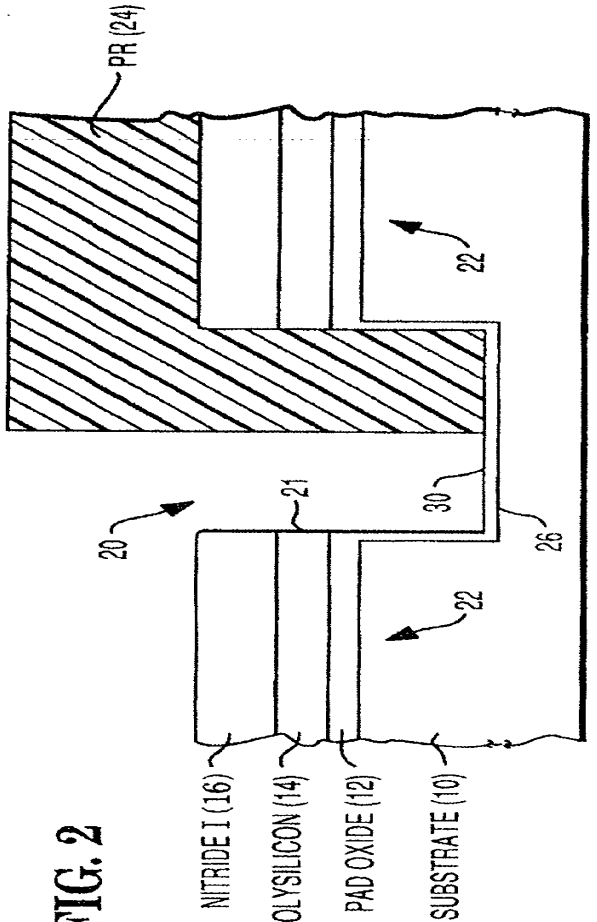
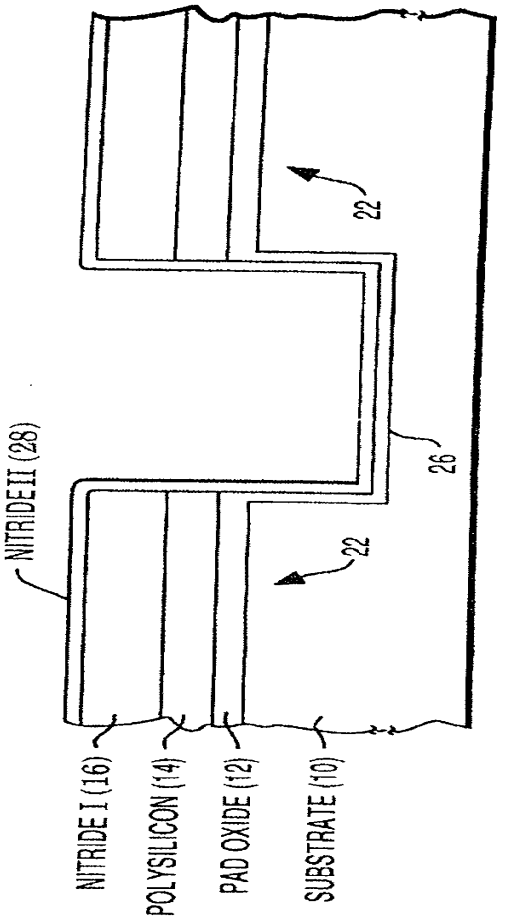

PR (24)
22
21
30
26
20
22
NITRIDE I (16)
POLYSILICON (14)
PAD OXIDE (12)
SUBSTRATE (10)

FIG. 2

FIG. 3


NITRIDE II (28)
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22
26
NITRIDE I (16)
POLYSILICON (14)
PAD OXIDE (12)
SUBSTRATE (10)

FIG. 4

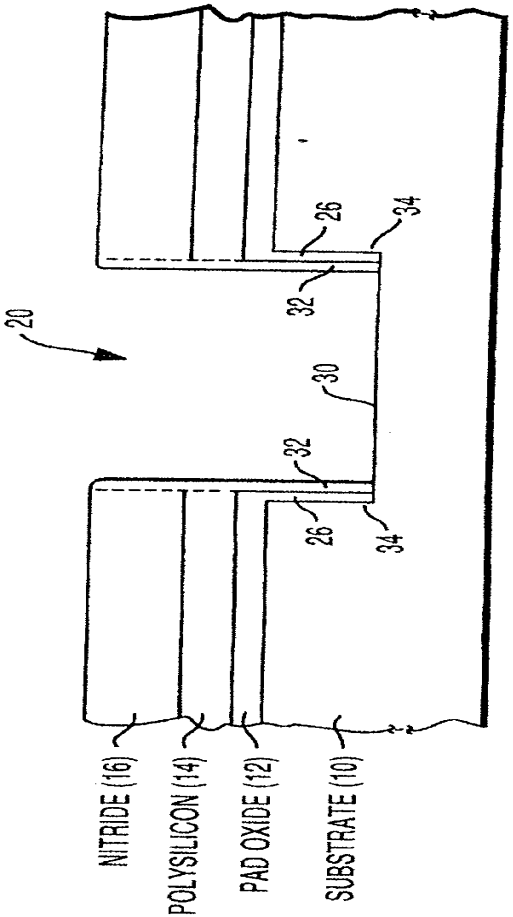

20
26
34
32
30
32
26
34
NITRIDE (16)
POLYSILICON (14)
PAD OXIDE (12)
SUBSTRATE (10)

FIG. 5

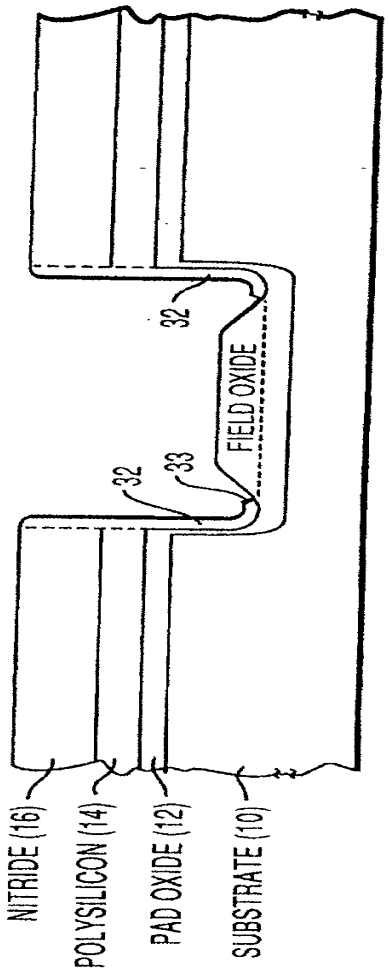
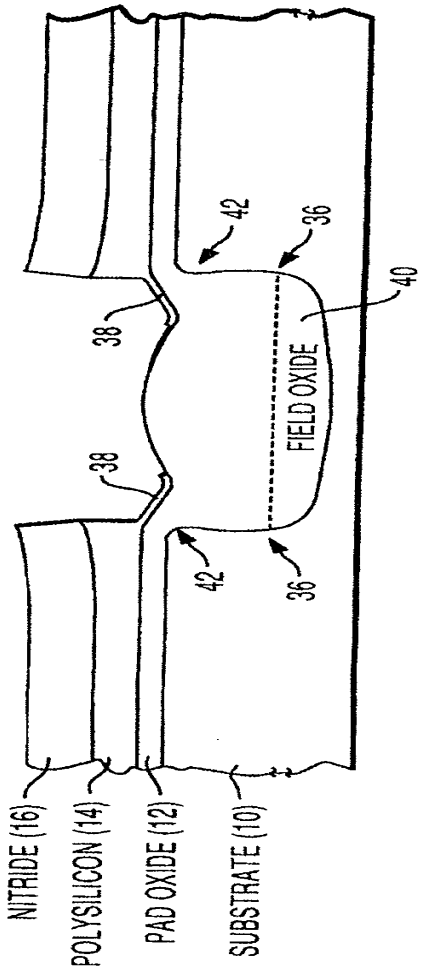

NITRIDE (16)
POLYSILICON (14)
PAD OXIDE (12)
SUBSTRATE (10)
32
33
32
FIELD OXIDE

FIG. 6


NITRIDE (16)
POLYSILICON (14)
PAD OXIDE (12)
SUBSTRATE (10)
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36
38
38
40
FIELD OXIDE
42
36

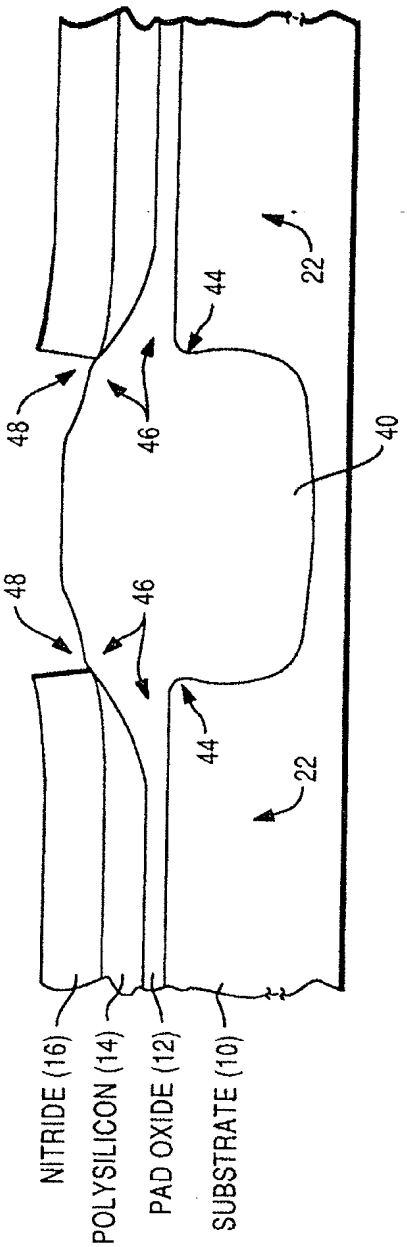
48
46
44
22
40
48
46
44
22
NITRIDE (16)
POLYSILICON (14)
PAD OXIDE (12)
SUBSTRATE (10)

FIG. 7

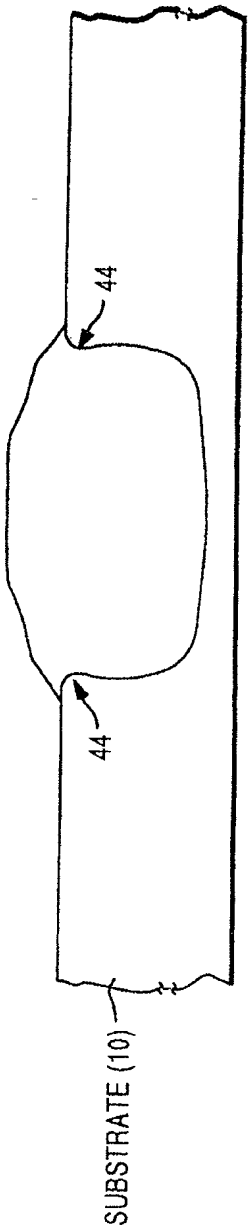
44
44
SUBSTRATE (10)

FIG. 8

FIG. 9

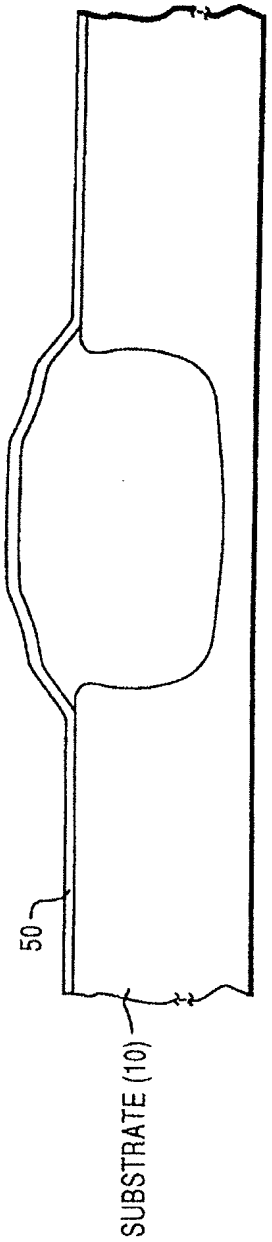

FIG. 10